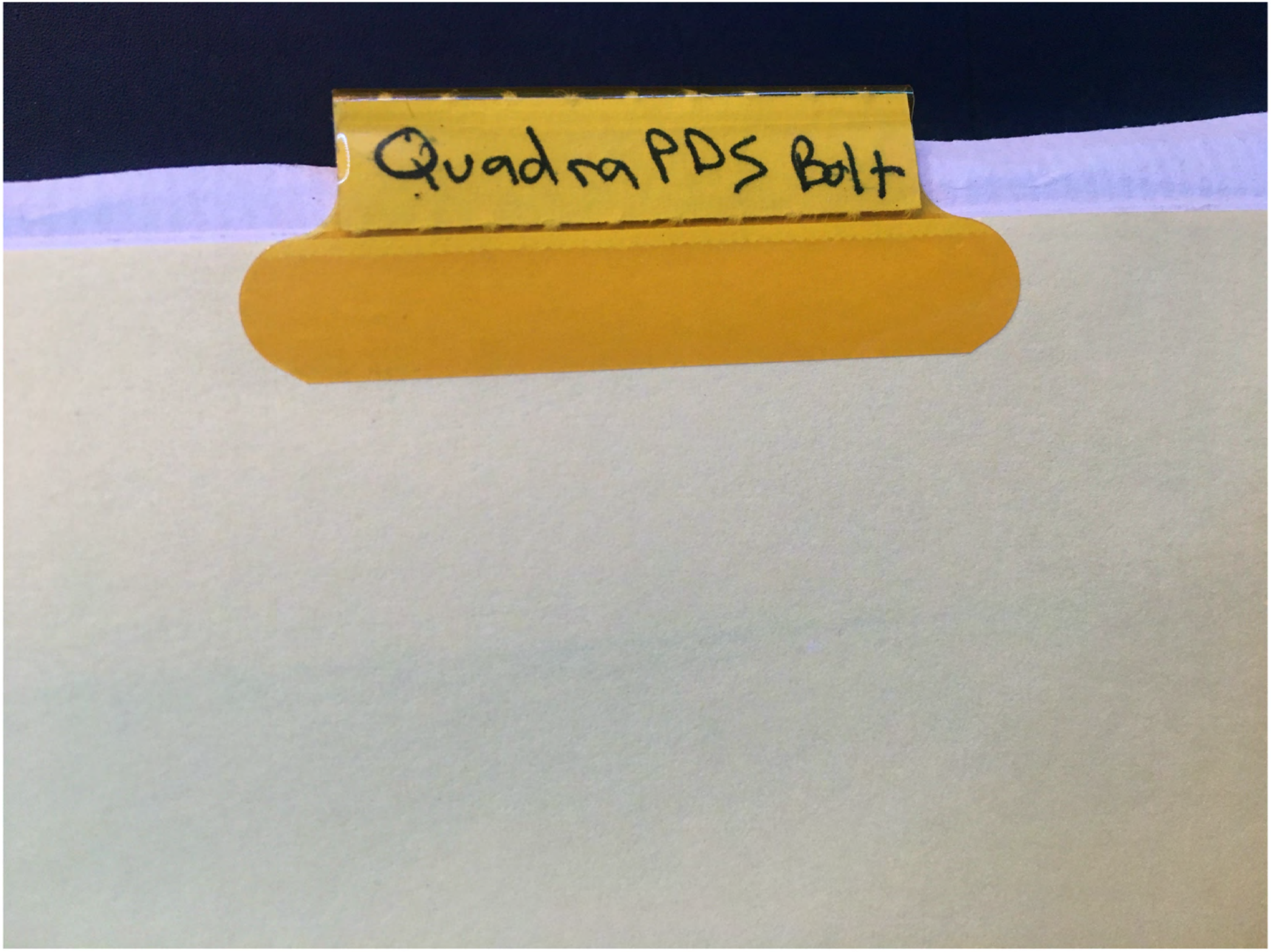
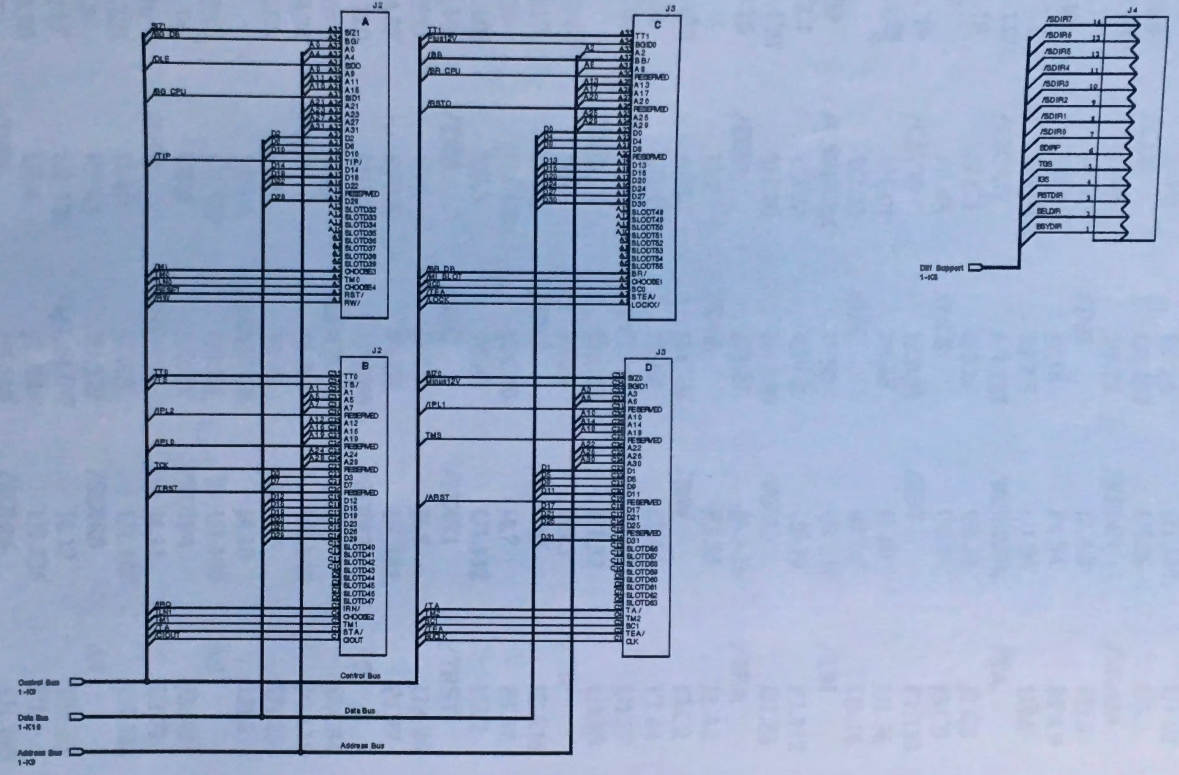

Quadra PDS Bolt

Daughter Board Connector
3x35 100-mil Headers, 2 places each



Title:	Daughter Board Connector
Project:	QuadraBoh3.0
Orig. Date:	2/18/93
By:	Karl Townsend
Mod. Date:	3/11/93 12:14 PM
By:	
Rev.:	A
Page	2 Of 2

Sixty Eight Thousand, Inc., 130 Technology Circle, Scotts Valley, CA 95066
Phone: (408) 438-1777 Fax: (408) 438-2997

/64K
H1.1
RP4.8
U3.10
/ACK
J1.38
RP2.2
U1.117
U5.18
/ARST
J3.C19
P1.127
/ATN
J1.32
RP2.4
U1.120
U5.16
/BB
J3.A32
P1.52
U1.98
/BG
P1.119
U2.15
/BG_710
U1.100
U2.16
/BG_CPU
J2.A27
P1.120
/BG_DB
J2.A34
U2.17
/BR
P1.51
U2.14
/BR_710
U1.101
U2.3
/BR_CPU
J3.A30
P1.50
/BR_DB
J3.A5
RP4.10
U2.4
/BSY
J1.36
RP2.3
U1.119
U5.17
/BUSERR
U2.20
U3.6
/CD
J1.46
RP1.4
U1.112
U5.25
/CIOUT
J2.C1
P1.48
/CS710
U1.93
U2.22
/CSPROM
U3.22
U4.20
/DB0
J1.2
RP3.7
U1.131
U5.2
/DB1
J1.4
RP3.6
U1.130
U5.3
/DB2
J1.6
RP3.5
U1.129
U5.4
/DB3
J1.8
RP3.4
U1.127
U5.5
/DB4
J1.10
RP3.3
U1.126
U5.6
/DB5
J1.12
RP3.2
U1.125
U5.10
/DB6
J1.14
RP2.7
U1.124
U5.11
/DB7
J1.16
RP2.6
U1.122
U5.12
/DBP
J1.18
RP2.5
U1.121
U5.13
/DLE
J2.A31
P1.45
/I/O
J1.50
RP1.2
U1.110
U5.27
/IPL0
J2.C26
P1.60
/IPL1
J3.C31
P1.61
/IPL2
J2.C30
P1.62
/IRQ
J2.C5
P1.58
U1.105
/LOCK
J3.A1
P1.53
/MASTER
U1.38
U2.23
/MI
J2.A5
P1.117
/MI_SLOT
J3.A4
P1.118
/MSG
J1.42
RP1.6
U1.115
U5.23
/OEPROM
U3.23
U4.22
/REQ
J1.48
RP1.3
U1.111
U5.26
/RESET
J2.A2
P1.54
U1.94
/ROMSEL
U2.21
U3.5
/RST
J1.40
RP1.7
U1.116
U5.19
/RSTO
J3.A26
P1.55
/RW
J2.A1
P1.41
U1.32
U3.3
/SDIR0
J4.7
U1.142
/SDIR1
J4.8
U1.141
/SDIR2
J4.9
U1.140
/SDIR3
J4.10
U1.138
/SDIR4
J4.11
U1.137
/SDIR5
J4.12
U1.135
/SDIR6
J4.13
U1.134
/SDIR7
J4.14
U1.133
/SEL
J1.44
RP1.5
U1.114
U5.24
/SLACK
U1.92
U3.4
/SRAM
H1.3
RP4.9
U3.8
/TA
J2.C2
J3.C5
P1.113
U1.36
U3.14
/TBI
P1.112
U1.35
/TEA
J3.A2
J3.C2
P1.44
U1.37
U3.15
/TIP
J2.A19
P1.42
U2.2
/TRST
J2.C20
P1.47
/TS
J2.C34
P1.115
U1.25
U3.2
A0
J2.A33
P1.72
U1.144
A1
J2.C33
P1.2
U1.145
A2
J3.A33
P1.73
U1.146
U4.10
A3
J3.C33
P1.3
U1.147
U4.9
A4
J2.A32
P1.4
U1.148
U4.8
A5
J2.C32
P1.75
U1.150
U4.7
A6
J3.C32
P1.5
U1.151
U4.6
A7
J2.C31
P1.6
U1.152
U4.5
A8
J3.A31
P1.77
U1.154
U4.4
A9
J2.A30
P1.7
U1.155
U4.3
A10
J3.C30
P1.78
U1.157
U4.25
A11
J2.A29
P1.8
U1.158
U4.24
A12
J2.C29
P1.79
U1.159
U4.21
A13
J3.A29
P1.9
U1.160
U4.23
A14
J3.C29

P1.80
U1.1
U4.2
A15
J2.A28
P1.10
U1.3
U4.26
A16
J2.C28
P1.81
U1.4
U3.7
A16/W
U3.21
U4.27
A17
J3.A28
P1.82
U1.5
U3.9
A18
J3.C28
P1.12
U1.7
A19
J2.C27
P1.13
U1.8
A20
J3.A27
P1.84
U1.10
A21
J2.A26
P1.14
U1.11
A22
J3.C26
P1.85
U1.12
A23
J2.A25
P1.15
U1.13
A24
J2.C25
P1.16
U1.14
U2.5
A25
J3.A25
P1.87
U1.16
U2.6
A26
J3.C25
P1.17
U1.17
U2.7
A27
J2.A24
P1.88
U1.18
U2.8
A28
J2.C24
P1.89
U1.20
U2.9
A29
J3.A24
P1.18
U1.21
U2.10
A30
J3.C24
P1.90
U1.23
U2.11
A31
J2.A23
P1.19
U1.24
U2.13
BSYDIR
J4.1
U1.108
BUCLK
J3.C1
P1.71
U1.41
U2.1
U3.1
D0
J3.A23
P1.109
U1.85
D1
J3.C23
P1.38
U1.84
D2
J2.A22
P1.108
U1.83
D3
J2.C22
P1.107
U1.81
D4
J3.A22
P1.36
U1.80
D5
J3.C22
P1.106
U1.78
D6
J2.A21
P1.35
U1.77
D7
J2.C21
P1.105
U1.76
D8
J3.A21
P1.34
U1.73
D9
J3.C21
P1.33
U1.72
D10
J2.A20
P1.103
U1.71
D11
J3.C20
P1.32
U1.70
D12
J2.C19
P1.102
U1.68
D13
J3.A19
P1.31
U1.67
D14
J2.A18
P1.30
U1.66
D15
J2.C18
P1.100
U1.65
D16
J3.A18
P1.99
U1.62
D17
J3.C18
P1.28
U1.60
D18
J2.A17
P1.98
U1.59
D19
J2.C17
P1.27
U1.58
D20
J3.A17
P1.97
U1.57
D21
J3.C17
P1.96
U1.56
D22
J2.A16
P1.25
U1.55
D23
J2.C16
P1.95
U1.53
D24
J3.A16
P1.24
U1.51
U4.11
D25
J3.C16
P1.23
U1.50
U4.12
D26
J2.C15
P1.93
U1.48
U4.13
D27
J3.A15
P1.22
U1.47
U4.15
D28
J2.A14
P1.92
U1.45
U4.16
D29
J2.C14
P1.21
U1.44
U4.17
D30
J3.A14
P1.91
U1.43
U4.18
D31
J3.C14
P1.20
U1.42
U4.19
DISCNCT
H2.2
U5.1
DP0
RP4.5
U1.86
DP1
RP4.4
U1.74
DP2
RP4.3
U1.63
DP3
RP4.2
U1.52
Ground
C1.2
C2.2
C3.2
C4.2
C5.2
C6.2
C7.2
C8.2
C9.2
C10.2
C11.2
C12.2
C13.2
C14.2
C15.2
C16.2
C17.2
C18.2
G1.7
H1.2
H2.1
J1.1
J1.3
J1.5
J1.7
J1.9
J1.11
J1.13
J1.15
J1.17
J1.19
J1.21
J1.23
J1.27
J1.29
J1.31
J1.33
J1.35
J1.37
J1.39
J1.41
J1.43
J1.45
J1.47
J1.49
J1.20
J1.22
J1.24
J1.28
J1.30
J1.34
J2.B1
J2.B3
J2.B5
J2.B7
J2.B9
J2.B11
J2.B13
J2.B15
J2.B17
J2.B19
J2.B21
J2.B23
J2.B25
J2.B27
J2.B29

J2.B31
J2.B33
J2.B35
J3.B1
J3.B3
J3.B5
J3.B7
J3.B9
J3.B11
J3.B13
J3.B15
J3.B17
J3.B19
J3.B21
J3.B23
J3.B25
J3.B27
J3.B29
J3.B31
J3.B33
J3.B35
P1.1
P1.11
P1.29
P1.39
P1.49
P1.59
P1.64
P1.76
P1.86
P1.94
P1.104
P1.114
P1.124
P1.132
RP1.1
RP2.1
RP3.1
U1.2
U1.9
U1.15
U1.22
U1.31
U1.46
U1.54
U1.61
U1.69
U1.75
U1.82
U1.91
U1.96
U1.109

U1.113
U1.118
U1.123
U1.128
U1.136
U1.143
U1.149
U1.156
U2.12
U3.11
U3.12
U3.13
U4.14
U5.7
U5.8
U5.9
U5.20
U5.21
U5.22
U5.28

IGS
J4.4
U1.104
ISCLK
G1.8
R1.1
ITERMPWR
D1.2
F1.2
Minus12V
J3.C34
P1.63
NOTERM
H2.3
RP4.7
PULLUP710
RP4.6
U1.87
U1.90
U1.95
Plus5V
C1.1
C2.1
C3.1
C4.1
C5.1
C6.1
C7.1
C8.1
C9.1
C10.1
C11.1

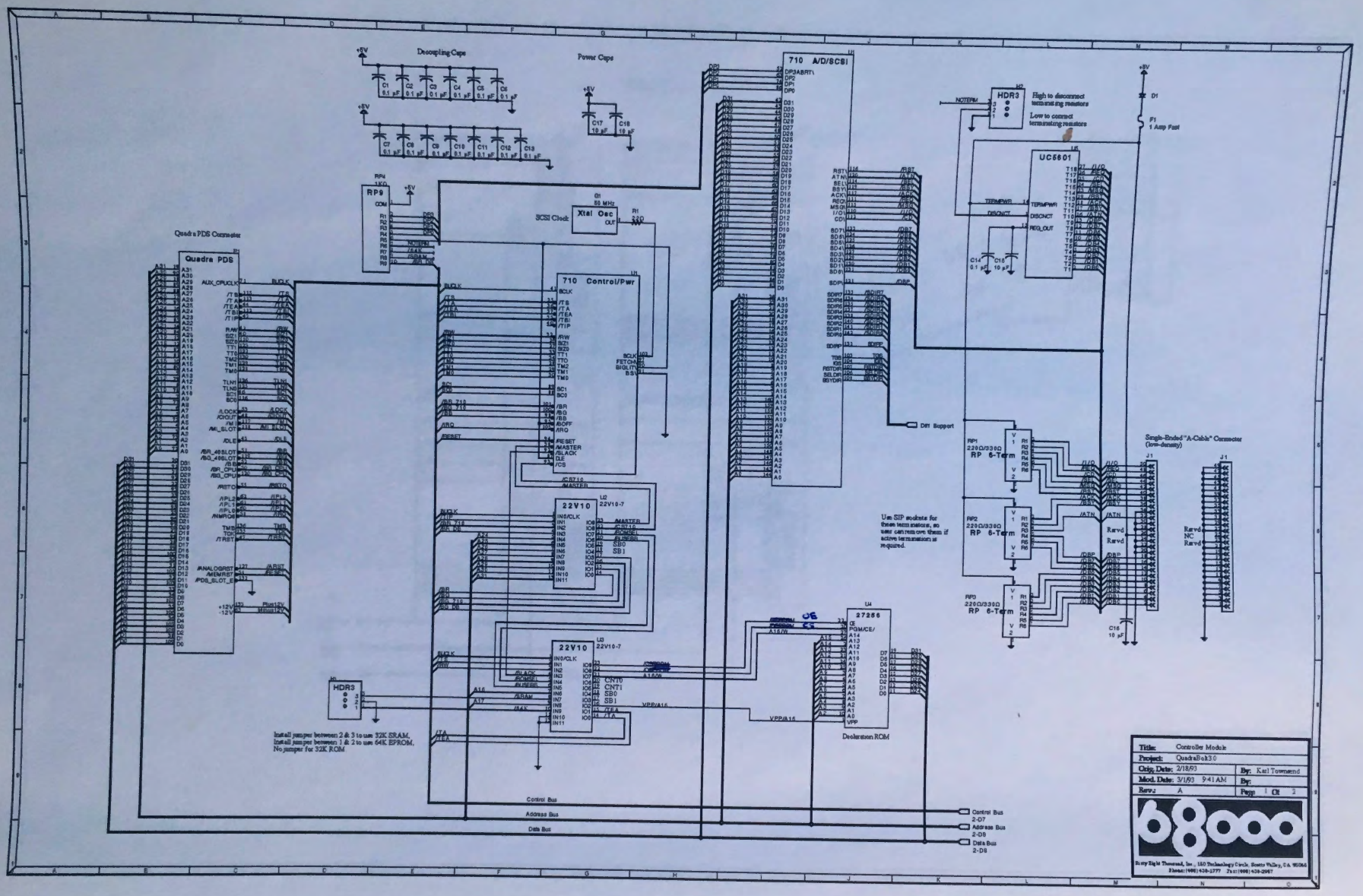
C12.1
C13.1
C17.1
C18.1
D1.1
G1.14
J2.B2
J2.B4
J2.B6
J2.B8
J2.B10
J2.B12
J2.B14
J2.B16
J2.B18
J2.B20
J2.B22
J2.B24
J2.B26
J2.B28
J2.B30
J2.B32
J2.B34
J3.B2
J3.B4
J3.B6
J3.B8
J3.B10
J3.B12
J3.B14
J3.B16
J3.B18
J3.B20
J3.B22
J3.B24
J3.B26
J3.B28
J3.B30
J3.B32
J3.B34
P1.26
P1.37
P1.56
P1.70
P1.74
P1.83
P1.101
P1.111
P1.121
P1.131
P1.140
RP4.1

U1.6
U1.19
U1.39
U1.49
U1.64
U1.79
U1.99
U1.139
U1.153
U2.24
U3.24
U4.28

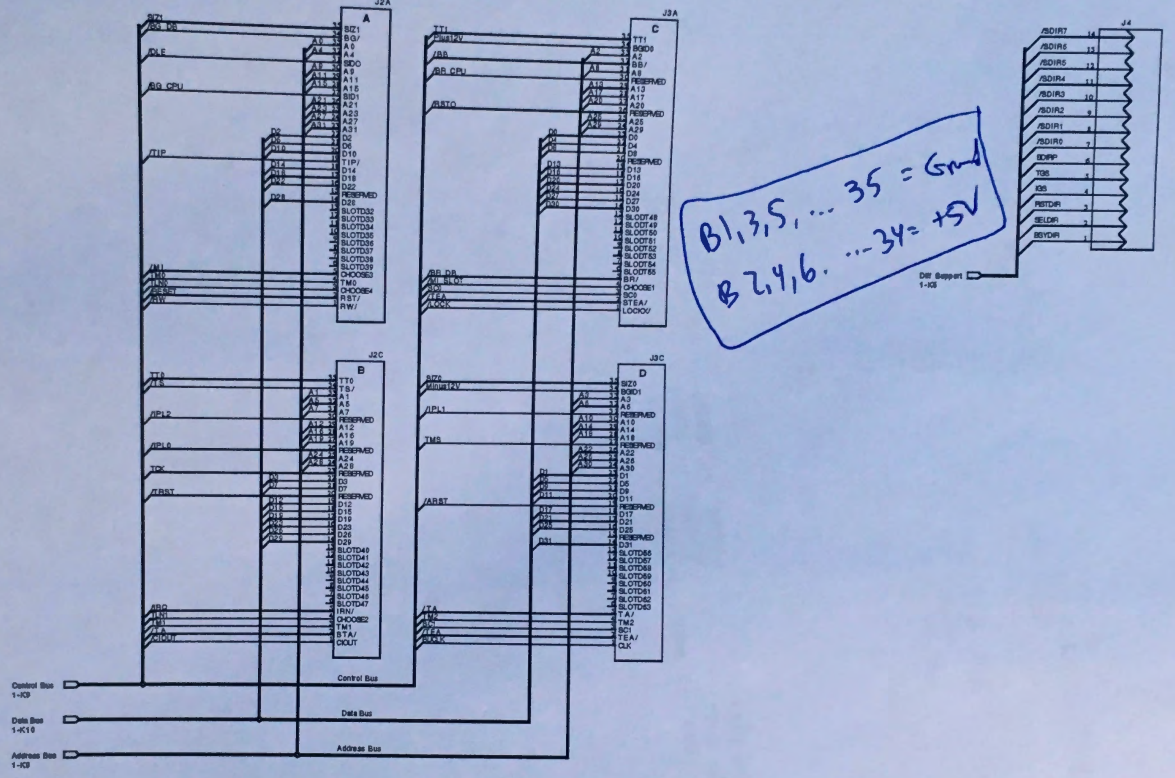
Plus12V
J3.A34
P1.133
REGOUT
C14.1
C15.1
U5.15
RSTDIR
J4.3
U1.107
SC0
J3.A3
P1.116
U1.88
SC1
J3.C3
P1.46
U1.89
SCLK
R1.2
U1.102
SDIRP
J4.6
U1.132
SELDIR
J4.2
U1.106
SIZ0
J3.C35
P1.110
U1.27
SIZ1
J2.A35
P1.40
U1.26
TCK
J2.C23
P1.135
TERMPWR
C16.1

F1.1
J1.26
RP1.8
RP2.8
RP3.8
U5.14
TGS
J4.5
U1.103
TLN0
J2.A3
P1.125
TLN1
J2.C4
P1.126
TM0
J2.A4
P1.128
U1.30
TM1
J2.C3
P1.129
U1.29
TM2
J3.C4
P1.130
U1.28
TMS
J3.C27
P1.136
TT0
J2.C35
P1.122
U1.34
TT1
J3.A35
P1.123
U1.33
VPP/A16
U3.16
U4.1

Rev. A


Decoupling Caps
Power Caps
710 A/D/SCSI
710 Control/Pwr
Quadra PDS Connector
Quadra PDS
SCSI Clock
Xtal Osc
HDR3
High to disconnect terminating resistors
Low to connect terminating resistors
UC5601
Diff Support
Single-Ended "A-Cable" Connector (low-density)
RP 6-Term
22V10
27256
Declaration ROM
Install jumper between 2 & 3 to use 32K SRAM.
Install jumper between 1 & 2 to use 64K EPROM.
No jumper for 32K ROM.
Control Bus
Address Bus
Data Bus
Control Bus 2-D7
Address Bus 2-D8
Data Bus 2-D8
Title: Controller Module
Project: QuadraBoard30
Orig. Date: 2/18/93
By: Karl Townsend
Mod. Date: 3/1/93 9:41 AM
Rev: A
Page 1 Of 2
Sixty Eight Thousand, Inc.

Daughter Board Connector
3x35 100-mil Headers, 2 places each



B1,3,5, ... 35 = Gnd
B 2,4,6. ... 34 = +5V

Title:	Daughter Board Connector		
Project:	QuadraBoh3.0		
Orig. Date:	2/18/93	By:	Karl Townsend
Mod. Date:	3/1/93 9:41 AM	By:	
Revs:	A	Page	2 Of 2

Sixty Eight Thousand, Inc., 160 Technology Circle, Scotts Valley, CA 95066
Phone: (408) 438-1777 Fax: (408) 438-2987

SIXTY EIGHT THOUSAND, INC.
100 Technology Circle, Scotts Valley, CA 95066

U2

```
module U2
title 'Quadra800 Built Address Decoder

Designer:    Karl A. Townsend
Company:     68000, Inc.
Date:        12-17-92
Rev.:        0'

U2   device  'P22V10';


"Inputs
     CLK,TIP,BR_710,BR_DB                    pin 1,2,3,4;
     A24,A25,A26,A27,A28,A29,A30,A31         pin 5,6,7,8,9,10,11,13;
     BG,MASTER                               pin 15,23;

"Outputs
     CS710,ROMSEL,BUSERR                     pin 22,21,20;
     SB0,SB1                                 pin 19,18;
     BR,BG_710,BG_DB                         pin 14,16,17;

     C,L,H,Z,X     = .C.,0,1,.Z.,.X.;

     ADDR    = [A31..A24];


equations

     !ROMSEL   = (!TIP # !MASTER) & (ADDR == ^hFE);          "All of Slot space is ROM
     !CS710    = (!TIP # !MASTER) & (ADDR == ^hEF);          "Top of Super Slot space is 710
     !BUSERR   = (!TIP # !MASTER) & (ADDR >= ^hE0) & (ADDR <= ^HEE);     "BUSERR anywhere else in
     Super Slot

     !BR       = !BR_710 # !BR_DB;
     !BG_710   = !BG;
     !BG_DB    =  BR_710 & !BR_DB & !BG & TIP & MASTER;
```

Phone: (408) 438-1777 Fax: (408) 438-2967 AppleLink: D1837

```
test_vectors

"1. Address Decoding

   ([ADDR,TIP]     ->    [ROMSEL,CS710,BUSERR])
    [^h00,0]       ->    [  1,     1,     1   ];
    [^h01,0]       ->    [  1,     1,     1   ];
    [^h10,0]       ->    [  1,     1,     1   ];
    [^h02,0]       ->    [  1,     1,     1   ];
    [^h20,0]       ->    [  1,     1,     1   ];
    [^hF0,0]       ->    [  1,     1,     1   ];
    [^hF8,0]       ->    [  1,     1,     1   ];
    [^h0F,0]       ->    [  1,     1,     1   ];
    [^hE0,0]       ->    [  1,     1,     0   ];
    [^hE4,0]       ->    [  1,     1,     0   ];
    [^hE8,0]       ->    [  1,     1,     0   ];
    [^hEE,0]       ->    [  1,     1,     0   ];
    [^hFE,0]       ->    [  0,     1,     1   ];
    [^hEF,0]       ->    [  1,     0,     1   ];


test_vectors

   ([CLK,BR_710,BR_DB,BG,TIP,MASTER] -> [BR,BG_710,BG_DB])

"15. 710 bus request
     [ C,   1,     1,  1,  1,   1   ] -> [ 1,    1,    1  ];
     [ C,   0,     1,  1,  1,   1   ] -> [ 0,    1,    1  ];
     [ C,   0,     1,  1,  1,   1   ] -> [ 0,    1,    1  ];
     [ C,   0,     1,  0,  1,   1   ] -> [ 0,    0,    1  ];
     [ C,   0,     1,  0,  1,   1   ] -> [ 0,    0,    1  ];
"    [ C,   1,     1,  0,  1,   1   ] -> [ 1,    1,    1  ];
     [ C,   1,     1,  1,  1,   1   ] -> [ 1,    1,    1  ];

"22. Daughter Board bus request
     [ C,   1,     1,  1,  1,   1   ] -> [ 1,    1,    1  ];
     [ C,   1,     0,  1,  1,   1   ] -> [ 0,    1,    1  ];
     [ C,   1,     0,  1,  1,   1   ] -> [ 0,    1,    1  ];
"    [ C,   1,     0,  0,  1,   1   ] -> [ 0,    1,    0  ];
"    [ C,   1,     0,  0,  1,   1   ] -> [ 0,    1,    0  ];
"    [ C,   1,     1,  0,  1,   1   ] -> [ 1,    1,    1  ];
     [ C,   1,     1,  1,  1,   1   ] -> [ 1,    1,    1  ];

"29. Both request
     [ C,   1,     0,  1,  1,   1   ] -> [ 0,    1,    1  ];
     [ C,   0,     0,  1,  1,   1   ] -> [ 0,    1,    1  ];
     [ C,   0,     0,  1,  1,   1   ] -> [ 0,    1,    1  ];
     [ C,   0,     0,  0,  1,   1   ] -> [ 0,    0,    1  ];
     [ C,   0,     0,  0,  1,   1   ] -> [ 0,    0,    1  ];
"    [ C,   1,     0,  0,  1,   1   ] -> [ 0,    1,    0  ];
"    [ C,   1,     0,  0,  1,   1   ] -> [ 0,    1,    0  ];
"    [ C,   1,     1,  0,  1,   1   ] -> [ 1,    1,    1  ];
     [ C,   1,     1,  1,  1,   1   ] -> [ 1,    1,    1  ];


end
```

ABEL 4.20 - Device Utilization Chart Tue Mar 9 09:44:24 1993

QuadraPDS Bolt Address Decoder

Designer: Karl A. Townsend
Company: 68000, Inc.
Date: 12-17-92
Rev.: 0

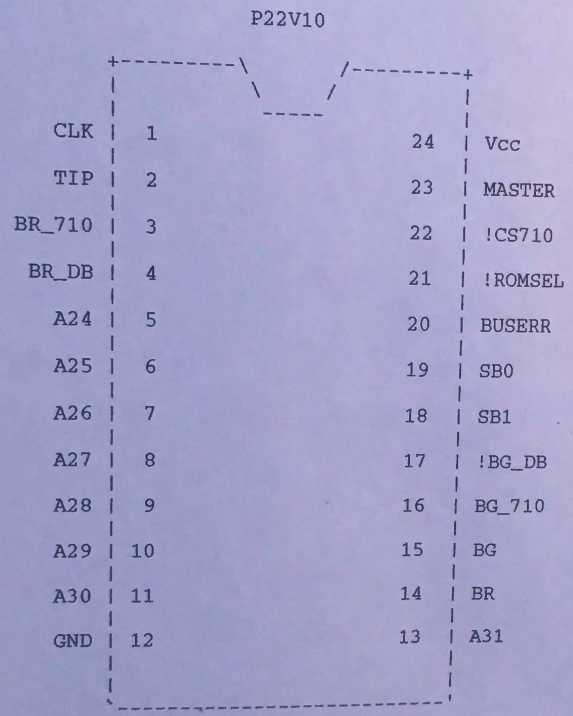
==== P22V10 Programmed Logic ====

```
ROMSEL      = !(  !A24 & A25 & A26 & A27 & A28 & A29 & A30 & A31 & !MASTER
                #   !TIP & !A24 & A25 & A26 & A27 & A28 & A29 & A30 & A31 );

CS710       = !(  A24 & A25 & A26 & A27 & !A28 & A29 & A30 & A31 & !MASTER
                #   !TIP & A24 & A25 & A26 & A27 & !A28 & A29 & A30 & A31 );

BUSERR      = (  TIP & MASTER
                #   !A31
                #   !A30
                #   !A29
                #   A28
                #   A24 & A25 & A26 & A27 );

BR      = (  BR_710 & BR_DB );

BG_710      = (  BG );

BG_DB       = !(  TIP & BR_710 & !BR_DB & !BG & MASTER );
```

QuadraPDS Bolt Address Decoder

Designer: Karl A. Townsend
Company: 68000, Inc.
Date: 12-17-92
Rev.: 0

==== P22V10 Chip Diagram ====



SIGNATURE: N/A

U3

```
module u3
title 'QuadraPDS Bolt ROM access controller

Designer:    Karl A. Townsend
Company:     68000, Inc.
Date:        12-17-92
Rev.:        0'

U3   device 'P22V10';


"Inputs
     CLK,TS,RW,SLACK,ROMSEL,BUSERR          pin 1,2,3,4,5,6;
     A16,SRAM,RESET                         pin 7,8,9;

"Outputs
     CSPROM,OEPROM,A16W                     pin 22,23,21;
     CNT0,CNT1,SB0,SB1                      pin 20,19,18,17 istype 'REG_D,buffer';
     VPPA16,TEA,TA                          pin 16,15,14;

     C,L,H,Z,X      = .C.,0,1,.Z.,.X.;

     CNT      = [CNT1,CNT0];

     ASTATE   = [SB1,SB0];
     S0       = ^b00;
     S1       = ^b10;
     S2       = ^b11;
     S3       = ^b01;

     PRELOAD = 3;                           "Change value for less wait states

equations

     !CSPROM = !ROMSEL;
     !OEPROM = !ROMSEL & RW;

     A16W     = A16 &  SRAM
              # RW  & !SRAM;
     VPPA16   =      SRAM
              # A16 & !SRAM;

     CNT     := (ASTATE == S1) & !ROMSEL & PRELOAD                          "Load Counter
              # (ASTATE == S2) & !ROMSEL & (CNT - 1) & (CNT != 0); "Decrement Counter

     !TEA    := !BUSERR & (ASTATE == S3);
      TEA.OE = !BUSERR;

     !TA     := !ROMSEL & (ASTATE == S2) & (CNT == 0)
              # !SLACK;
      TA.OE   = !ROMSEL;


state_diagram (ASTATE)

     State S0: "Idle State
            IF !TS THEN S1
            ELSE S0;

     State S1: "Wait for decode
            IF !BUSERR THEN S3
            ELSE IF !ROMSEL THEN S2
            ELSE S0;

     State S2: "Wait for CNT = 0
            IF (CNT == 0) THEN S3
            ELSE S2;
```

```
    State S3: "Assert TA
            GOTO S0;


test_vectors ([CLK,RESET,TS,RW,ROMSEL,BUSERR,SLACK,SRAM,A16]
            -> [ASTATE,CSPROM,OEPROM,A16W,VPPA16,CNT,TA,TEA])

"1. This file assumes no RESET and PAL powers on with flip flops cleared
"     [C,0,X,X,X,X,X,X,X]       ->    [S0,1,1,X,X,0,Z,Z]; Reset
      [C,1,1,X,1,1,1,X,X]       ->    [S0,1,1,X,X,0,Z,Z]; "Do nothing

"3. 710 Accesses
      [C,1,0,X,1,1,1,X,X]       ->    [S1,1,1,X,X,0,Z,Z]; "Wait for decode
      [C,1,1,X,1,1,1,X,X]       ->    [S0,1,1,X,X,0,Z,Z]; "Back to S0

"5. Bus Errors
      [C,1,0,X,1,1,1,X,X]       ->    [S1,1,1,X,X,0,Z,Z]; "Wait for decode
      [C,1,1,X,1,0,1,X,X]       ->    [S3,1,1,X,X,0,Z,1]; "BUSERR
      [C,1,1,X,1,0,1,X,X]       ->    [S0,1,1,X,X,0,Z,0]; "Back to S0, Assert TEA
      [C,1,1,X,1,1,1,0,X]       ->    [S0,1,1,X,X,0,Z,Z]; "Stay in S0

"8. ROM Read
      [C,1,0,X,1,1,1,1,X]       ->    [S1,1,1,X,X,0,Z,Z]; "Wait for decode
      [C,1,1,1,0,1,1,1,0]       ->    [S2,0,0,0,1,3,1,Z]; "Load Counter
      [C,1,1,1,0,1,1,1,0]       ->    [S2,0,0,0,1,2,1,Z]; "Wait for CNT = 0
      [C,1,1,1,0,1,1,1,1]       ->    [S2,0,0,1,1,1,1,Z]; "Wait for CNT = 0
      [C,1,1,1,0,1,1,1,1]       ->    [S2,0,0,1,1,0,1,Z]; "Wait for CNT = 0
      [C,1,1,X,0,1,1,X,X]       ->    [S3,0,1,X,X,0,0,Z]; "Assert TA
      [C,1,1,X,1,1,1,X,X]       ->    [S0,1,1,X,X,0,Z,Z]; "Back to S0

"15. ROM Write, nothing happens
      [C,1,0,X,1,1,1,1,X]       ->    [S1,1,1,X,X,0,Z,Z]; "Wait for decode
      [C,1,1,0,0,1,1,1,0]       ->    [S2,0,1,0,1,3,1,Z]; "Load Counter
      [C,1,1,0,0,1,1,1,0]       ->    [S2,0,1,0,1,2,1,Z]; "Wait for CNT = 0
      [C,1,1,0,0,1,1,1,1]       ->    [S2,0,1,1,1,1,1,Z]; "Wait for CNT = 0
      [C,1,1,0,0,1,1,1,1]       ->    [S2,0,1,1,1,0,1,Z]; "Wait for CNT = 0
      [C,1,1,X,0,1,1,1,X]       ->    [S3,0,1,X,X,0,0,Z]; "Assert TA
      [C,1,1,X,1,1,1,1,X]       ->    [S0,1,1,X,X,0,Z,Z]; "Back to S0

"22. SRAM Read
      [C,1,0,X,1,1,1,0,X]       ->    [S1,1,1,X,X,0,Z,Z]; "Wait for decode
      [C,1,1,1,0,1,1,0,0]       ->    [S2,0,0,1,0,3,1,Z]; "Load Counter
      [C,1,1,1,0,1,1,0,0]       ->    [S2,0,0,1,0,2,1,Z]; "Wait for CNT = 0
      [C,1,1,1,0,1,1,0,1]       ->    [S2,0,0,1,1,1,1,Z]; "Wait for CNT = 0
      [C,1,1,1,0,1,1,0,1]       ->    [S2,0,0,1,1,0,1,Z]; "Wait for CNT = 0
      [C,1,1,X,0,1,1,0,X]       ->    [S3,0,1,X,X,0,0,Z]; "Assert TA
      [C,1,1,X,0,1,1,0,X]       ->    [S0,0,1,X,X,0,1,Z]; "Back to S0
      [C,1,1,X,1,1,1,0,X]       ->    [S0,1,1,X,X,0,Z,Z]; "Stay in S0

"29. SRAM Write
      [C,1,0,X,1,1,1,0,X]       ->    [S1,1,1,X,X,0,Z,Z]; "Wait for decode
      [C,1,1,0,0,1,1,0,0]       ->    [S2,0,1,0,0,3,1,Z]; "Load Counter
      [C,1,1,0,0,1,1,0,0]       ->    [S2,0,1,0,0,2,1,Z]; "Wait for CNT = 0
      [C,1,1,0,0,1,1,0,1]       ->    [S2,0,1,0,1,1,1,Z]; "Wait for CNT = 0
      [C,1,1,0,0,1,1,0,1]       ->    [S2,0,1,0,1,0,1,Z]; "Wait for CNT = 0
      [C,1,1,X,0,1,1,0,X]       ->    [S3,0,1,X,X,0,0,Z]; "Assert TA
      [C,1,1,X,1,1,1,0,X]       ->    [S0,1,1,X,X,0,Z,Z]; "Back to S0

end
```

QuadraPDS Bolt ROM access controller

Designer: Karl A. Townsend
Company: 68000, Inc.
Date: 12-17-92
Rev.: 0

==== P22V10 Programmed Logic ====

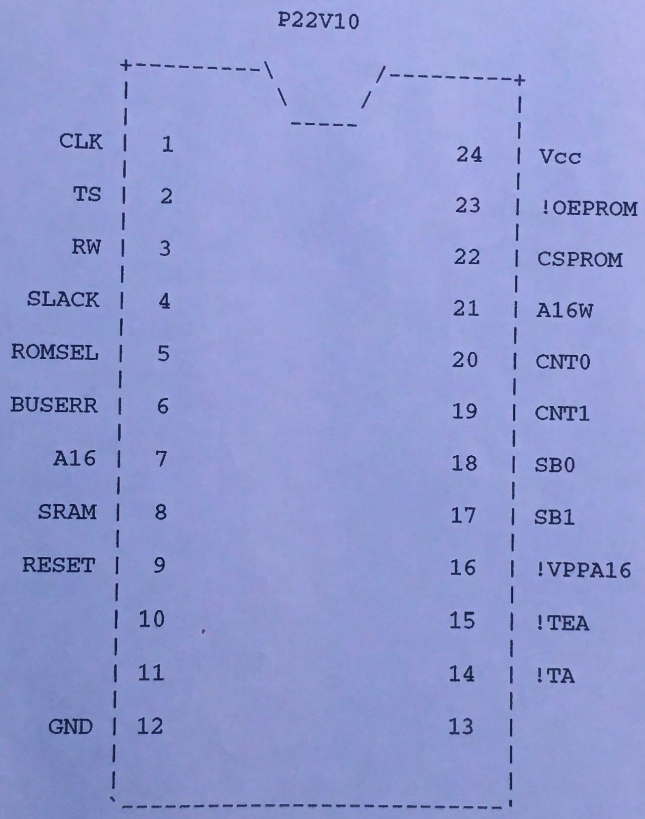
```
CSPROM      = (  ROMSEL );

OEPROM      = !(  RW & !ROMSEL );

A16W        = (  RW & !SRAM
              #   A16 & SRAM );

VPPA16      = !(  !A16 & !SRAM );

CNT1.D      = (  !ROMSEL & CNT0 & CNT1 & SB1
              #   !ROMSEL & !SB0 & SB1 ); " ISTYPE 'BUFFER'

CNT0.D      = (  !ROMSEL & !SB0 & SB1
              #   !ROMSEL & !CNT0 & CNT1 & SB1 ); " ISTYPE 'BUFFER'

TEA.D       = (  !BUSERR & SB0 & !SB1 ); " ISTYPE 'INVERT'
TEA.OE      = (  !BUSERR );

TA.D        = (  !ROMSEL & !CNT0 & !CNT1 & SB0 & SB1
              #   !SLACK ); " ISTYPE 'INVERT'
TA.OE       = (  !ROMSEL );

SB0.D       = (  SB0.Q & SB1.Q
              #   !BUSERR & SB1.Q
              #   !ROMSEL & SB1.Q ); " ISTYPE 'BUFFER'

SB1.D       = (  !ROMSEL & BUSERR & !SB0.Q & SB1.Q
              #   !TS & !SB0.Q & !SB1.Q
              #   CNT1 & SB0.Q & SB1.Q
              #   CNT0 & SB0.Q & SB1.Q ); " ISTYPE 'BUFFER'
```

Warning 5087: Mapping SB0 to SB0.FB; only one fb is allowed on pin 18
Warning 5087: Mapping SB1 to SB1.FB; only one fb is allowed on pin 17

QuadraPDS Bolt ROM access controller Tue Mar 9 09:45:18 1993

Designer: Karl A. Townsend
Company: 68000, Inc.
Date: 12-17-92
Rev.: 0

==== P22V10 Chip Diagram ====



SIGNATURE: N/A

Bill Of Materials
QuadraBolt3.0 Monday, March 1, 1993 3:25 PM

Count	Part	Value	Rating	Package	Ref. Des.
1	1N5817		1 Amp	Axial-400mil	D1
2	22V10-7			DIP24	U2 U3
1	27C256	7 ns	10ns	DIP28	U4
1	53C710	200 ns	120ns	PQFP160	U1
4	581-10M10	10 µF	16 WVDC	Thruhole	C15 C16 C17 C18
14	581-UDZ104K1	0.1 µF	16 WVDC	Thruhole	C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14
1	8807-140-170LH			KEL 140-pin	P1
1	Fuse		1 Amp Fast	5x20mm Glass	F1
2	Hdr3			.025 sq-100mil	H1 H2
1	Hdr14			1x14-100mil	J4
1	Hdr50			2x25-100mil	J1
4	Hdr105			3x35-100mil	J2A J2C J3A J3C
3	RP-6 Term	220Ω/330Ω		SIP8	RP1 RP2 RP3
1	RP-9 Pullup	1KΩ		SIP10	RP4
1	Res	22Ω	1/8 W	Thruhole	R1
1	UC5601DWP			SOIC28	U5
1	XO-43B-50	50 MHz	CMOS	DIP14	G1

Sockets Required:

Count	Socket	Package	Ref. Des.
3	SIP8	SIP8	RP1 RP2 RP3
2	DIP24	DIP24	U2 U3
1	DIP28	DIP28	U4
1	Fuse Holder	5x20mm Glass	F1
1	XTAL	DIP14	G1

TERMPWR	C16.1 RP3.8	F1.1 U5.14	J1.26	RP1.8	RP2.8
/TA	J2.C2	J3.C5	P1.113	U1.36	U3.14
/TEA	J3.A2	J3.C2	P1.44	U1.37	U3.15
BUCLK	J3.C1	P1.71	U1.41	U2.1	U3.1
/ACK	J1.38	RP2.2	U1.117	U5.18	
/ATN	J1.32	RP2.4	U1.120	U5.16	
/BSY	J1.36	RP2.3	U1.119	U5.17	
/CD	J1.46	RP1.4	U1.112	U5.25	
/DB0	J1.2	RP3.7	U1.131	U5.2	
/DB1	J1.4	RP3.6	U1.130	U5.3	
/DB2	J1.6	RP3.5	U1.129	U5.4	
/DB3	J1.8	RP3.4	U1.127	U5.5	
/DB4	J1.10	RP3.3	U1.126	U5.6	
/DB5	J1.12	RP3.2	U1.125	U5.10	
/DB6	J1.14	RP2.7	U1.124	U5.11	
/DB7	J1.16	RP2.6	U1.122	U5.12	
/DBP	J1.18	RP2.5	U1.121	U5.13	
/I/O	J1.50	RP1.2	U1.110	U5.27	
/MSG	J1.42	RP1.6	U1.115	U5.23	
/REQ	J1.48	RP1.3	U1.111	U5.26	
/RST	J1.40	RP1.7	U1.116	U5.19	
/RW	J2.A1	P1.41	U1.32	U3.3	
/SEL	J1.44	RP1.5	U1.114	U5.24	
/TS	J2.C34	P1.115	U1.25	U3.2	
A2	J3.A33	P1.73	U1.146	U4.10	
A3	J3.C33	P1.3	U1.147	U4.9	
A4	J2.A32	P1.4	U1.148	U4.8	
A5	J2.C32	P1.75	U1.150	U4.7	
A6	J3.C32	P1.5	U1.151	U4.6	
A7	J2.C31	P1.6	U1.152	U4.5	
A8	J3.A31	P1.77	U1.154	U4.4	
A9	J2.A30	P1.7	U1.155	U4.3	
A10	J3.C30	P1.78	U1.157	U4.25	

A11	J2.A29	P1.8	U1.158	U4.24
A12	J2.C29	P1.79	U1.159	U4.21
A13	J3.A29	P1.9	U1.160	U4.23
A14	J3.C29	P1.80	U1.1	U4.2
A15	J2.A28	P1.10	U1.3	U4.26
A16	J2.C28	P1.81	U1.4	U3.7
A17	J3.A28	P1.82	U1.5	U3.9
A24	J2.C25	P1.16	U1.14	U2.5
A25	J3.A25	P1.87	U1.16	U2.6
A26	J3.C25	P1.17	U1.17	U2.7
A27	J2.A24	P1.88	U1.18	U2.8
A28	J2.C24	P1.89	U1.20	U2.9
A29	J3.A24	P1.18	U1.21	U2.10
A30	J3.C24	P1.90	U1.23	U2.11
A31	J2.A23	P1.19	U1.24	U2.13
D24	J3.A16	P1.24	U1.51	U4.11
D25	J3.C16	P1.23	U1.50	U4.12
D26	J2.C15	P1.93	U1.48	U4.13
D27	J3.A15	P1.22	U1.47	U4.15
D28	J2.A14	P1.92	U1.45	U4.16
D29	J2.C14	P1.21	U1.44	U4.17
D30	J3.A14	P1.91	U1.43	U4.18
D31	J3.C14	P1.20	U1.42	U4.19
PULLUP710	RP4.6	U1.87	U1.90	U1.95
/64K	H1.1	RP4.8	U3.10	
/BB	J3.A32	P1.52	U1.98	
/BR_DB	J3.A5	RP4.10	U2.4	
/IRQ	J2.C5	P1.58	U1.105	
/RESET	J2.A2	P1.54	U1.94	
/SRAM	H1.3	RP4.9	U3.8	
/TIP	J2.A19	P1.42	U2.2	
A0	J2.A33	P1.72	U1.144	
A1	J2.C33	P1.2	U1.145	

A18	J3.C28	P1.12	U1.7
A19	J2.C27	P1.13	U1.8
A20	J3.A27	P1.84	U1.10
A21	J2.A26	P1.14	U1.11
A22	J3.C26	P1.85	U1.12
A23	J2.A25	P1.15	U1.13
D0	J3.A23	P1.109	U1.85
D1	J3.C23	P1.38	U1.84
D2	J2.A22	P1.108	U1.83
D3	J2.C22	P1.107	U1.81
D4	J3.A22	P1.36	U1.80
D5	J3.C22	P1.106	U1.78
D6	J2.A21	P1.35	U1.77
D7	J2.C21	P1.105	U1.76
D8	J3.A21	P1.34	U1.73
D9	J3.C21	P1.33	U1.72
D10	J2.A20	P1.103	U1.71
D11	J3.C20	P1.32	U1.70
D12	J2.C19	P1.102	U1.68
D13	J3.A19	P1.31	U1.67
D14	J2.A18	P1.30	U1.66
D15	J2.C18	P1.100	U1.65
D16	J3.A18	P1.99	U1.62
D17	J3.C18	P1.28	U1.60
D18	J2.A17	P1.98	U1.59
D19	J2.C17	P1.27	U1.58
D20	J3.A17	P1.97	U1.57
D21	J3.C17	P1.96	U1.56
D22	J2.A16	P1.25	U1.55
D23	J2.C16	P1.95	U1.53
REGOUT	C14.1	C15.1	U5.15
SC0	J3.A3	P1.116	U1.88
SC1	J3.C3	P1.46	U1.89

SIZ0	J3.C35	P1.110	U1.27
SIZ1	J2.A35	P1.40	U1.26
TM0	J2.A4	P1.128	U1.30
TM1	J2.C3	P1.129	U1.29
TM2	J3.C4	P1.130	U1.28
TT0	J2.C35	P1.122	U1.34
TT1	J3.A35	P1.123	U1.33
/ARST	J3.C19	P1.127	
/BG	P1.119	U2.15	
/BG_710	U1.100	U2.16	
/BG_CPU	J2.A27	P1.120	
/BG_DB	J2.A34	U2.17	
/BR	P1.51	U2.14	
/BR_710	U1.101	U2.3	
/BR_CPU	J3.A30	P1.50	
/BUSERR	U2.20	U3.6	
/CIOUT	J2.C1	P1.48	
/CS710	U1.93	U2.22	
/CSPROM	U3.22	U4.20	
/DLE	J2.A31	P1.45	
/IPL0	J2.C26	P1.60	
/IPL1	J3.C31	P1.61	
/IPL2	J2.C30	P1.62	
/LOCK	J3.A1	P1.53	
/MASTER	U1.38	U2.23	
/MI	J2.A5	P1.117	
/MI_SLOT	J3.A4	P1.118	
/OEPROM	U3.23	U4.22	
/ROMSEL	U2.21	U3.5	
/RSTO	J3.A26	P1.55	
/SDIR0	J4.7	U1.142	
/SDIR1	J4.8	U1.141	
/SDIR2	J4.9	U1.140	

/SDIR3	J4.10	U1.138
/SDIR4	J4.11	U1.137
/SDIR5	J4.12	U1.135
/SDIR6	J4.13	U1.134
/SDIR7	J4.14	U1.133
/SLACK	U1.92	U3.4
/TBI	P1.112	U1.35
/TRST	J2.C20	P1.47
A16/W	U3.21	U4.27
BSYDIR	J4.1	U1.108
DISCNCT	H2.2	U5.1
DP0	RP4.5	U1.86
DP1	RP4.4	U1.74
DP2	RP4.3	U1.63
DP3	RP4.2	U1.52
IGS	J4.4	U1.104
ISCLK	G1.8	R1.1
ITERMPWR	D1.2	F1.2
Minus12V	J3.C34	P1.63
NOTERM	H2.3	RP4.7
Plus12V	J3.A34	P1.133
RSTDIR	J4.3	U1.107
SCLK	R1.2	U1.102
SDIRP	J4.6	U1.132
SELDIR	J4.2	U1.106
TCK	J2.C23	P1.135
TGS	J4.5	U1.103
TLN0	J2.A3	P1.125
TLN1	J2.C4	P1.126
TMS	J3.C27	P1.136
VPP/A16	U3.16	U4.1